IN THE CLAIMS:

Rewrite the pending claims as follows:

1. (Currently amended) A circuit for generating an output signal with a predetermined duty cycle, comprising:

a driver that generates an output signal;

a detector coupled to the driver, ~~the detector configured~~ to determine a common mode voltage of the output signal;

a comparator coupled to the detector~~, the comparator configured~~ to compare the common mode voltage of the output signal to a reference voltage for a predetermined duty cycle;

a register coupled to the comparator~~, the register configured~~ to store a value indicative of a difference between the common mode voltage of the output signal and the reference voltage;

adjustment combining logic to combine a second value and the value stored in the register to produce an adjusted value; and

a pre-driver ~~coupled to the register, the pre-driver configured~~ to receive a signal corresponding to the adjusted value ~~derived at least in part from the value stored in the register~~ and to send a data signal corresponding to the output signal to the driver, wherein the value stored in the register causes the common mode voltage of the output signal to change so as to decrease the difference between the common mode voltage of the output signal and the reference voltage.

2. (Original) The circuit of claim 1, wherein the common mode voltage of the output signal becomes substantially equal to the reference voltage through a plurality of iterations through a closed loop.

3. (Original) The circuit of claim 1, wherein the duty cycle of the generated output signal takes into account variations due to packaging.

4. (Original) The circuit of claim 1, wherein the output signal is a symmetric pattern.

5. (Original) The circuit of claim 1, further comprising a counter coupled between the comparator and the register.

6. (Original) The circuit of claim 1, further comprising a digital-to-analog converter coupled between the register and the pre-driver.

7. (Original) The circuit of claim 6, wherein an analog voltage from the digital-to-analog converter configures the pre-driver.

8. (Original) The circuit of claim 6, wherein an output of the digital-to-analog converter is coupled to a gate of a transistor of the pre-driver.

9. (Currently Amended) The circuit of claim 1, further comprising:

a first digital-to-analog converter coupled between the register and the pre-driver, wherein an output of the first digital-to-analog converter is coupled to a first gate of a first transistor of the pre-driver; and

a second register coupled to the comparator~~, the second register configured~~ to store a value indicative of a difference between the common mode voltage of the output signal and the reference voltage; and

a second digital-to-analog converter coupled between the second register and the pre-driver, wherein an output of the second digital-to-analog converter is coupled to a second gate of a second transistor of the pre-driver.

10. (Original) The circuit of claim 1, further comprising a plurality of registers coupled to the comparator, each of the registers configured to store a value that configures the pre-driver to generate an output signal for a respective duty cycle of respective one of a plurality of signal types.

11. (Currently Amended) The circuit of claim 1, further comprising an input ~~configured~~ to receive an externally provided value, the externally provided value comprising the second value.~~, and adjustment combining logic configured to combine the externally provided value and the value stored in the register to produce an adjusted value; wherein the signal received by the pre-driver corresponds to the adjusted value.~~

12. (Currently Amended) The circuit of claim 1, further comprising a process/voltage/temperature (PVT) detector to produce a signal corresponding to the second value.~~, and adjustment combining logic configured to combine a value from the PVT detector~~

~~and the value stored in the register to produce an adjusted value; wherein the signal received by the pre-driver corresponds to the adjusted value.~~

13. (Currently Amended) The circuit of claim 12, wherein the signal produced by ~~value from~~ the PVT detector is a digital code.

14. (Original) The circuit of claim 12, wherein the PVT detector comprises a delay lock loop (DLL).

15. (Original) The circuit of claim 12, wherein the PVT detector includes a frequency detector to track operating frequency.

16. (Currently Amended) The circuit of claim 12, further comprising an input ~~configured~~ to receive an externally provided value, wherein the adjustment combining logic is configured to combine the externally provided value, the second value ~~from the PVT detector~~ and the value stored in the register to produce the adjusted value; and wherein the signal received by the pre-driver corresponds to the adjusted value.

17. (Currently Amended) The circuit of claim 1, further comprising a frequency detector to track operating frequency to produce a signal corresponding to the second value.~~, and adjustment combining logic configured to combine a value from the frequency detector and the value stored in the register to produce an adjusted value; wherein the signal received by the pre-driver corresponds to the adjusted value.~~

18. (Currently Amended) A method of generating an output signal with a predetermined duty cycle, comprising:

determining a common mode voltage of an output signal;

comparing the common mode voltage of the output signal to a reference voltage for a predetermined duty cycle;

storing in a register a value indicative of a difference between the common mode voltage of the output signal and the reference voltage;

combining a second value and the value stored in the register to produce an adjusted value; and

re-configuring a pre-driver, used in generating the output signal, in accordance with the adjusted value ~~stored in the register~~ so as to cause a decrease in the difference between the common mode voltage of the output signal and the reference voltage.

19. (Currently Amended) The method of claim 18, further comprising repeating the determining, comparing, storing, combining and re-configuring through a plurality of iterations.

20. (Currently Amended) The method of claim 18, wherein re-configuring comprises:

converting of the adjusted value ~~in the register~~ from a digital value to an analog signal; and

applying the analog signal to a gate of a transistor of the pre-driver.

21. (Original) The method of claim 18, further comprising selecting a register from a plurality of registers, each register storing a value suitable for configuring the pre-driver to generate an output signal with a duty cycle of one of a plurality of signaling types.

22. (Currently Amended) The method of claim 18, wherein the second value is ~~further comprising re-configuring the pre-driver in accordance with~~ an externally provided value.

~~23.~~ (Currently Amended ) The method of claim 18, wherein the second value is ~~further comprising combining the value stored in the register with~~ a value obtained from a process/voltage/temperature (PVT) detector. ~~to generate a combined value;~~

~~wherein the re-configuring includes re-configuring the pre-driver in accordance with the combined value.~~

24. (Currently Amended) The method of claim 23, further including combining the value stored in the register with [[a]] the value obtained from a process/voltage/temperature (PVT) detector and an externally provided value to produce the combined value.

25. (Original) The method of claim 18, wherein the second value is ~~further including combining the value stored in the register with~~ a value obtained from a frequency detector. ~~to produce a combined value that tracks an operating frequency.~~

26. (Currently Amended) A system, comprising:

a first circuit ~~configured~~ to receive signals of a specific signaling type, the specific signaling type having a predetermined duty cycle; and

a second circuit coupled to the first circuit, the second circuit comprising:

a pre-driver;

a plurality of registers coupled to the pre-driver, each register ~~configured~~ to store a value suitable for configuring the pre-driver to generate an output signal with a duty cycle of one of a plurality of signaling types, wherein the specific signaling type is one of the plurality of signaling types; and

a selector, coupled to the plurality of registers, ~~the selector configured~~ to select one of the plurality of registers so as to output the value stored in the selected register;

wherein the pre-driver is configured in accordance with the output value from the selected register so as to generate an output signal with the predetermined duty cycle and send the output signal to the first circuit.

27. (Currently Amended) The system of claim 26, wherein the second circuit further comprises:

a driver coupled to the pre-driver~~, the driver configured~~ to generate the output signal;

a detector coupled to the driver~~, the detector configured~~ to determine a common mode voltage of the output signal;

a comparator coupled to the detector~~, the comparator configured~~ to compare the common mode voltage of the output signal to a reference voltage for the duty cycle of selected signaling type of the plurality of signaling types; and

the plurality of registers coupled to the comparator, each respective register of the plurality of registers storing a value indicative of a difference between the common mode voltage of the output signal and a respective reference voltage for the duty cycle of a respective one of the plurality of signaling types.

28. (Original) The system of claim 27, further comprising a counter coupled between the comparator and the plurality of registers.

29. (Original) The system of claim 26, further comprising a digital-to-analog converter coupled between the plurality of registers and the pre-driver.

30. (Original) The system of claim 29, wherein an analog signal from the digital-to-analog converter configures the pre-driver.

31. (Original) The system of claim 29, wherein an analog signal from the digital-to-analog converter is coupled to a gate of a transistor of the pre-driver.

32. (Currently Amended) The system of claim 26, further comprising an input ~~configured~~ to receive an externally provided value and adjustment combining logic ~~configured~~ to combine the externally provided value and a value stored in the selected register to produce an adjusted value; wherein the pre-driver is configured in accordance with the adjusted value.

33. (Currently Amended l) The system of claim 26, further comprising a process/voltage/temperature (PVT) detector, and adjustment combining logic ~~configured~~ to combine a value from the PVT detector and a value stored in the selected register to produce an adjusted value; wherein the pre-driver is configured in accordance with the adjusted value.

34. (Original) The system of claim 33, wherein the value from the PVT detector is a digital code.

35. (Original) The system of claim 33, wherein the PVT detector comprises a delay lock loop (DLL).

36. (Original) The system of claim 33, wherein the PVT detector includes a frequency detector to track operating frequency.

37. (Currently Amended) The system of claim 33, further comprising an input ~~configured~~ to receive externally provided values for storage in the plurality of registers.

38. (Currently Amended) The system of claim 26, further comprising a frequency detector to track operating frequency, and adjustment combining logic ~~configured~~ to combine a value from the frequency detector and the value stored in the selected register to produce an adjusted value; wherein the pre-driver is configured in accordance with the adjusted value.

39. (Currently amended) A method of generating an output signal for one of a plurality of signaling types, comprising:

selecting one of a plurality of registers, each respective register storing a value suitable for configuring a pre-driver to generate an output signal with a duty cycle of a respective signaling type of [[a]] the plurality of signaling types; and

configuring the pre-driver according to the selected register, the pre-driver generating an output signal with a duty cycle ~~substantially equal to the duty cycle of the respective signaling type~~ corresponding to the value stored in the selected register.

40. (Original) The method of claim 39, including receiving input specifying the selected register or specifying the signaling type corresponding to the value stored in the selected register.

41. (Original) The method of claim 39, wherein configuring comprises:
converting of the value in the register from a digital value to an analog signal; and
applying the analog signal to a gate of a transistor of the pre-driver.

42. (Original) The method of claim 39, further comprising receiving an externally provided value, combining the value stored in the selected register with the externally provided value to produce an adjusted value, and configuring the pre-driver in accordance with the adjusted value.

43. (Original) The method of claim 39, further including combining the value stored in the selected register with a value obtained from a process/voltage/temperature (PVT) detector to produce a combined value, and configuring the pre-driver in accordance with the combined value.

44. (Original) The method of claim 43, including combining the value stored in the register with the value obtained from the process/voltage/temperature (PVT) detector and an externally provided value to produce a combined value, and configuring the pre-driver in accordance with the combined value.

45. (Original) The method of claim 43, wherein the PVT detector includes a frequency detector and the value obtained from the PVT detector tracks an operating frequency.

46. (Original) The method of claim 39, further including combining the value stored in the selected register with a value obtained from a frequency detector to produce a combined value that tracks an operating frequency, and configuring the pre-driver in accordance with the combined value.